ABSTRACT

~~A data recovery system for a serial digital data link includes a data sampler, compare logic, a phase controller, and a phase shifter. The data sampler samples input data three times in a bit time which time is determined by clock pulses generated by the phase shifter, and recovers digital data according to a predetermined decision criterion. Data sampling phases are split so as to track the data eye. The compare logic compares the output of the data sampler according to a predetermined method. Phase controller uses the output of the compare logic and generates phase control signals. These signals are set so as to control the sampling times of the data sampler and to attain near optimally recovered data stream. The phase shifter uses the phase control signals and makes three different phase clocks from input clock. The input clock can be an external clock, or can be recovered from the external clock or input data stream.~~An exemplary embodiment of a data recovery apparatus for a digital data stream of input data optionally includes a phase shifter that outputs multiple sampling clocks in a bit time, where the phase of said sampling clocks are automatically adjustable and a data sampler that samples the input data using the sampling clocks as triggers, and for providing multiple sampled data signals, where one of said sampled data signals is used to output recovered data. Also optionally included can be compare logic that compares said sampled data signals to said recovered data and an optional phase controller for estimating the phase relationship between the input data and said sampling clocks using the comparison result of said compare logic, and for providing control signals to said phase controller according to said estimation result.